



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,857	03/30/2004	Kwang Won Koh	4459-142	2343

7590

09/09/2005

LOWE HAUPTMAN GILMAN & BERNER, LLP  
Suite 310  
1700 Diagonal Road  
Alexandria, VA 22314

EXAMINER
----------

POTTER, ROY KARL

ART UNIT	PAPER NUMBER
----------	--------------

2822

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/811,857

Applicant(s)

KOH ET AL.

Examiner

Roy K. Potter

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on 11 August 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 14-20 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8-13 is/are allowed.
- 6) ☒ Claim(s) 1,2 and 7 is/are rejected.
- 7) ☒ Claim(s) 3-6 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Election/Restrictions***

Applicant's election with traverse of claims 1 - 13 in the reply filed on 8/11/2005 is acknowledged. The traversal is on the ground(s) that examination of the entire application can be made without a serious burden. This is not found persuasive because these inventions are distinct for the reasons provided in the Restriction Requirement and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes is proper.

The requirement is still deemed proper and is therefore made FINAL.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 2 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Mclellan et al..

Mclellan et al., U.S. Patent No. 6,229,200 discloses a SAW singulated leadless plastic chip carrier. As described in column 4, beginning on line 28, lead frame 201 includes die attach pad 202 and lead 203, shown in Figure 2b, for example. The thickness is described as being 0.13 mm in line 41 of column 4. A first semiconductor die 206 is attached to the die attach pad 202 and electrically coupled to leads 203 by

Art Unit: 2822

wires 205. A package body 401 is formed over the semiconductor device so that the lower surfaces of the die pad and the leads are exposed through the package body. IN column 4, line 44 explains that any suitable adhesive can be used to attach the die to the die attach pad, and soft solder is described as one of these suitable adhesives.

In regard to claim 7, as explained in column 6, beginning on line 7, the lead frame is provided with interlocking lip 507 to enhance the locking of the leads and die pad in the package body.

***Allowable Subject Matter***

Claims 8 – 13 are allowed.

The prior art does not teach or suggest first and second die pads, an output bar and leads exposed through the package body.

The prior art also does not teach or suggest the leadless chip package comprising first and second die pads having a thickness of 10 to 20 mils.

Claims 3 – 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art does not teach or suggest the recited output bar connected by a heavy aluminum wire.

The prior art also does not teach or suggest the recited second die pad disposed between the leads and a second semiconductor device.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cheah et al., U.S. Patent No. 6448643, discloses a semiconductor package. As shown in figure 5, the package includes multiple die pads and multiple semiconductor devices located on the die pads.

Bayan et al., U.S. Patent No. 6452255 discloses a low inductance leadless package. As shown in Figure 6F, the package comprises a first die pad 207 and a plurality of leads 209 arranged around the periphery of the die pad 207. A first semiconductor device 220 is attached to the upper surface of the die pad 207 and electrically coupled to the leads by wires 222. A package body 225 is formed over the semiconductor device 220 and the leads 209 in such a manner that the lower surface of the leads 209 are exposed through the package. Bayan et al. discloses that the die attach adhesive 211 attaches the semiconductor device 220 to the die pad 207, but does not disclose that the die attach adhesive is.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roy K. Potter whose telephone number is 308 - 4106. The examiner can normally be reached on M-F.

Art Unit: 2822

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Roy K Potter  
Primary Examiner  
Art Unit 2822